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ANALYSIS OF DATAPATH FOR POWER, AREA, AND THROUGHPUT

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ABSTRACT

In this paper we a representing a power efficient high throughput data path architectures. There are few previously proposed architectures which will also give the same results but we have modified such that it provides higher power efficiency and large area. In this paper, we have shown two different data path arrangements for signed and unsigned operations. The expected outcome is to find the feasible design that will reduce the complexity and improve the performance. The circuits have been systematically designed to reduce power consumption.

KEYWORDS: *Datapath Elements, Computer Architecture Organization, Dataflow*

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